Amendments to the Claims:

The following listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Previously Presented) A semiconductor device comprising:

a semiconductor substrate having a P-type well;

an N-type MOS transistor which is formed on the semiconductor substrate to pull down a pad to a ground level and includes a first N-type diffusion region connected to the pad;

a first isolation region which isolates the N-type MOS transistor from other adjacent MOS transistors on the semiconductor substrate;

a second isolation region formed between the N-type MOS transistor and the first isolation region;

a second N-type diffusion region which is formed in a region isolated by the second isolation region from the N-type MOS transistor and makes up a lateral bipolar transistor together with the P-type well in the semiconductor substrate and the first N-type diffusion region of the N-type MOS transistor;

a first P-type diffusion region which is formed at a deeper position of the first N-type diffusion region near the second isolation region and makes up a Zener diode by the PN junction together with the first N-type diffusion region of the N-type MOS transistor;

a second P-type diffusion region which is isolated by a third isolation region from the second N-type diffusion region;

a silicide layer formed on a surface of the semiconductor substrate excluding the first to third isolation regions; and

a ground terminal which is connected to the second N-type diffusion region and the second P-type diffusion region through the silicide layer.

2. (Previously Presented) The semiconductor device as defined in claim 1,

wherein the impurity concentration of the first P-type diffusion region is set to a value enabling a breakdown start voltage of the Zener diode to be lower than a breakdown start voltage of the N-type MOS transistor.

3-4. (Canceled)

5. (Previously Presented) The semiconductor device as defined in claim 1, further comprising:

a third N-type diffusion region which is provided between the silicide layer and the first P-type diffusion region and makes up a Schottky diode together with the silicide layer.

6. (Previously Presented) The semiconductor device as defined in claim 1, further comprising:

a third P-type diffusion region and a third N-type diffusion region formed between the silicide layer and the first P-type diffusion region,

wherein the first and third P-type diffusion regions and the third N-type diffusion region make up a PNP bipolar transistor.

7-19. (Canceled)

20. (Currently Amended) A semiconductor device comprising:

a semiconductor substrate having a P-type well;

an N-type MOS transistor which is formed on the semiconductor substrate to pull down a pad to a ground level and includes a first N-type diffusion region connected to the pad;

a first isolation region which isolates the N-type MOS transistor from other adjacent MOS transistors on the semiconductor substrate;

a second isolation region formed between the N-type MOS transistor and the first isolation region;

a second N-type diffusion region which is formed in a region isolated by the second isolation region from the N-type MOS transistor and makes up a lateral bipolar transistor together with the P-type well in the semiconductor substrate and the first N-type diffusion region of the N-type MOS transistor;

a first P-type diffusion region which is formed between the second isolation region and the first N-type diffusion region and near a surface of the semiconductor substrate and makes up a Zener diode by the PN junction together with the first N-type diffusion region of the N-type MOS transistor;

a second P-type diffusion region which is isolated by a third isolation~~N-type diffusion~~ region from the second N-type diffusion region;

a silicide layer formed on a surface of the semiconductor substrate excluding the first to third isolation regions and a region connecting the first N-type diffusion region and first P-type diffusion region; and

a ground terminal which is connected to the second N-type diffusion region and the second P-type diffusion region through the silicide layer.

21. (Previously Presented) The semiconductor device as defined in claim 20,

wherein the impurity concentration of the first P-type diffusion region is set to a value enabling a breakdown start voltage of the Zener diode to be lower than a breakdown start voltage of the N-type MOS transistor.

22-26. (Canceled)

27. (Previously Presented) The semiconductor device as defined in claim 1, further comprising:

a P-type MOS transistor which is formed on the semiconductor substrate to pull up the pad to a ground level and includes a third P-type diffusion region connected to the pad through a resistance;

a fourth P-type diffusion region isolated by a fourth isolation region from the third P-type diffusion region; and

a third N-type diffusion region formed lower than the fourth isolation region and between the third and fourth P-type diffusion regions,

wherein the pad is connected to the fourth P-type diffusion region and the third N-type diffusion region functions as the resistance.

28. (Previously Presented) The semiconductor device as defined in claim 27 further comprising:

a fourth N-type diffusion region provided in a region surrounded by the silicide layer, third N-type diffusion region, fourth isolation region and fourth P-type diffusion region and makes up a Schottky diode together with the silicide layer,

wherein the silicide layer is formed on a surface of the fourth P-type diffusion region.

Amendments to the Drawings:

The attached replacement drawing sheets make changes to Figs. 1, 22, 23, 24 and 28 and replace the original sheets with Figs. 1, 22, 23, 24 and 28.

Attachment: Replacement Sheets